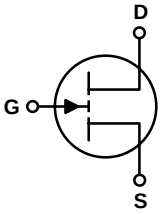
INN100W032B

1. General description

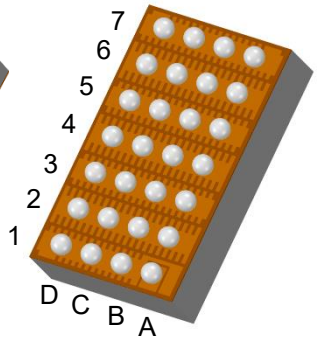
GaN-on-Silicon enhancement mode high-electron-mobility-transistor (HEMT) in Solder Ball WLCSP with 3.5 mm x 2.13 mm package size.



2. Features

- GaN-on-Silicon E-mode HEMT technology
- Very low gate charge
- Ultra-low on resistance
- Very small package size
- Zero reverse recovery charge

Top View



Bottom View

3. Applications

- Synchronous rectification
- Class-D audio
- High frequency DC-DC converter
- Communication base station
- Motor driver

4. Key performance parameters

Table 1 Key performance parameters at T_J = 25 °C

Parameter	Value	Unit
$V_{DS,max}$	100	V
$R_{DS(on),max}$ @ V_{GS} = 5 V	3.2	mΩ
$Q_{G,typ}$ @ V_{DS} = 50V	9.2	nC
$I_{DS,Pulse}$ (T_A = 25 °C)	230	A
Q_{OSS}@ V_{DS} = 50V	50	nC

5. Pin information

Table 2 Pin information

PIN	Pin Description	Pin Function
A3/A5/A7/B1/B3/B5/B7/C1/C3/C5/C7/D1/D3/D5/D7	Source	Power Source
A2/A4/A6/B2/B4/B6/C2/C4/C6/D2/D4/D6	Drain	Power Drain
A1	Gate	Driver Gate

Table 3 Ordering information

Type/Ordering Code	Package	Product Code
INN100W032B	WLCSP 3.5x2.13	J38

Table of contents

6. Maximum ratings

at T_J = 25 °C unless otherwise specified.

Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact Innoscience sales office.

Table 4 Maximum ratings

SYMBOL	PARAMETER	MAX	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
$V_{DS(tr)}$	Drain-to-Source Voltage [1] (V_{GS}=0V, 1h total time, T_A=T_{JMAX})	120	V
I_D	Continuous current (T_C = 25 °C, $R_{\theta JC}$=0.68 ˚C/W)	165	A
	Continuous current (T_C = 100 °C, $R_{\theta JC}$=0.68 ˚C/W)	105	A
	Continuous current (T_A = 25 °C, $R_{\theta JA}$=39.86 ˚C/W)[2]	22	A
	Pulsed (T_A = 25˚C, T_{PULSE} = 300 µs)	230	A
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	V
T_J	Operating Temperature	-40 to 150	˚C
T_{STG}	Storage Temperature	-40 to 150	˚C

Note:

1. Provided as measure of robustness under abnormal operating conditions and not recommended for normal operation;
2. $R_{\theta JA}$ is determined with the device on FR4 PCB (2s2p with thermal vias) defined in accordance with JEDEC standards. PCB is mounted in horizontal position without air stream cooling.

7. Thermal characteristics

Table 5 Thermal characteristics

SYMBOL	PARAMETER	TYP	UNIT	Note/Test Condition
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.68	˚C/W	
$R_{\theta JB}$	Thermal Resistance, Junction to Board	4.64	˚C/W	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient [2]	39.86	˚C/W	
T_{sold}	Maximum reflow soldering temperature	260	°C	MSL1

8. Electric characteristics

at T_J = 25 °C unless otherwise specified.

Table 6 Static characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
I_{DSS}	Drain Source Leakage	-	4	28	μA	V_{GS} = 0 V, V_{DS} =80 V
I_{GSS}	Gate-to-Source Forward Leakage(25°C)	-	1.2	23	μA	V_{GS} = 5 V
	Gate-to-Source Forward Leakage(125°C)		0.1	2	mA	V_{GS} = 5 V
	Gate-to-Source Reverse Leakage	-	0.1	0.5	μA	V_{GS} = -4 V
$V_{GS(TH)}$	Gate Threshold Voltage	0.8	1.1	2.5	V	V_{DS} = V_{GS}, I_D = 9 mA
$R_{DS(on)}$	Drain-Source On-state Resistance [3]	-	2.5	3.2	mΩ	V_{GS} = 5 V, I_D = 25 A
V_{SD}	Source-Drain Forward Voltage	-	1.5	-	V	I_S = 0.5 A, V_{GS} = 0 V

Note:

3. $R_{DS(on)}$ is measured without prior drain bias or switching stress.

Table 7 Dynamic characteristics [4]

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{ISS}	Input Capacitance	-	1000	-	pF	V_{GS} = 0 V, V_{DS} = 50 V
C_{OSS}	Output Capacitance	-	460	-		V_{GS} = 0 V, V_{DS} = 50 V
C_{RSS}	Reverse Transfer Capacitance	-	8.2	-		V_{GS} = 0 V, V_{DS} = 50 V
$C_{OSS(ER)}$	Energy Related C_{OSS}	-	700	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
$C_{OSS(TR)}$	Time Related C_{OSS}	-	1020	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
R_G	Gate resistance	-	1.9	-	Ω	f = 5 MHz, open drain
Q_G	Total Gate Charge	-	9.2	12	nC	V_{GS} = 5 V, V_{DS} = 50 V, I_D= 25 A
Q_{GS}	Gate to Source Charge	-	1.9	-		V_{DS} = 0 V to 50 V, I_D = 25 A
Q_{GD}	Gate to Drain Charge	-	1.7	-		V_{DS} = 0 V to 50 V, I_D = 25 A
$Q_{G(TH)}$	Gate Charge at Threshold	-	1.1	-		V_{DS} = 0 V to 50 V, I_D = 25 A
Q_{OSS}	Output Charge	-	50	-		V_{GS} = 0 V, V_{DS} = 0 V to 50 V
Qrr	Reverse recovery charge	-	0	-		V_{DS} = 50 V, I_S = 25 A

Note:

4. Guaranteed by design.

9. Electric characteristics diagrams

at T_J = 25 °C unless otherwise specified.

Fig. 1 Typical Output Characteristics (T_J=25°C)

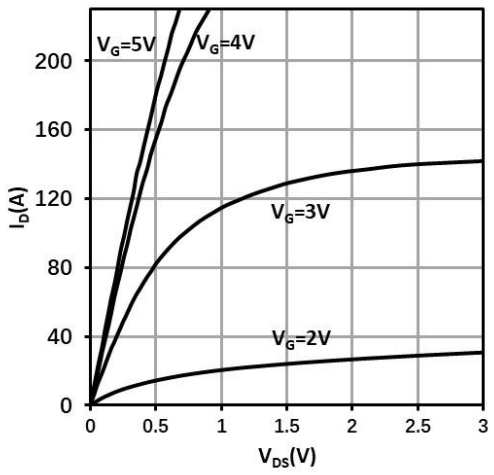


Fig. 2 Typical Output Characteristics (T_J=125°C)

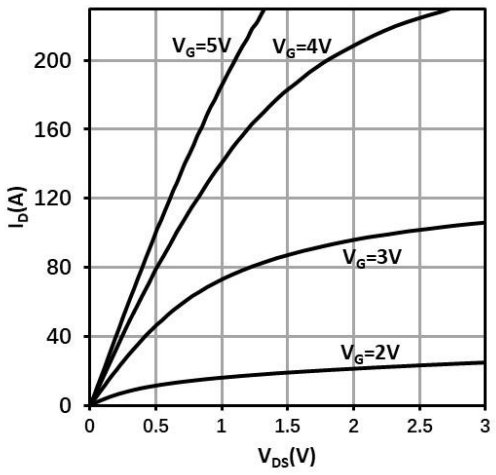


Fig. 3 Typical Drain On-state Resistance (T_J=25°C)

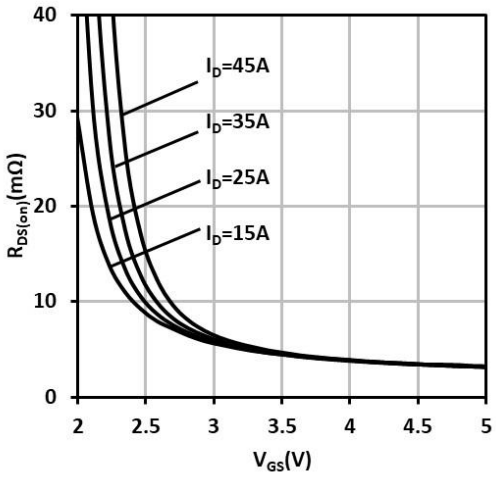


Fig. 4 Typical Drain On-state Resistance (T_J=125°C)

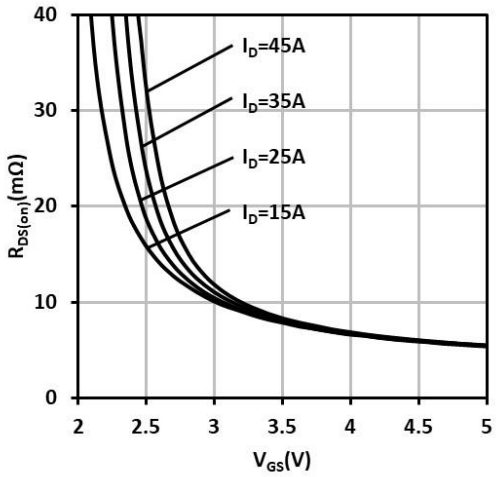


Fig. 5 Normalized On-State Resistance vs. Temp.

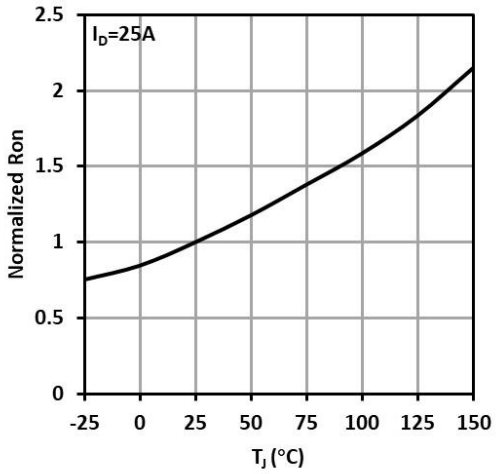


Fig. 6 Typical Transfer Characteristics

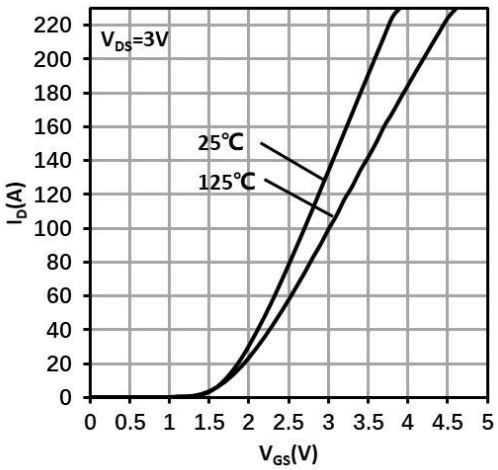


Fig. 7 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0, T_J$=25°C)

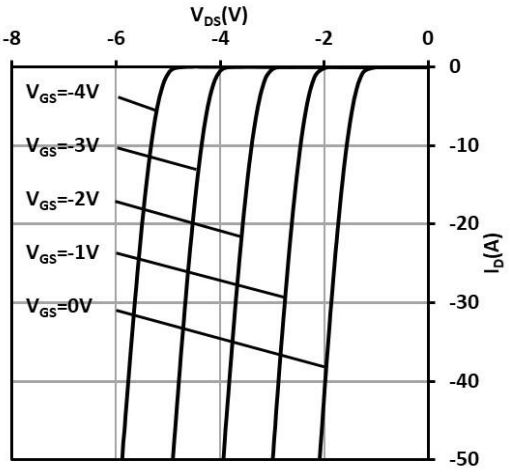


Fig. 8 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0, T_J$=25°C)

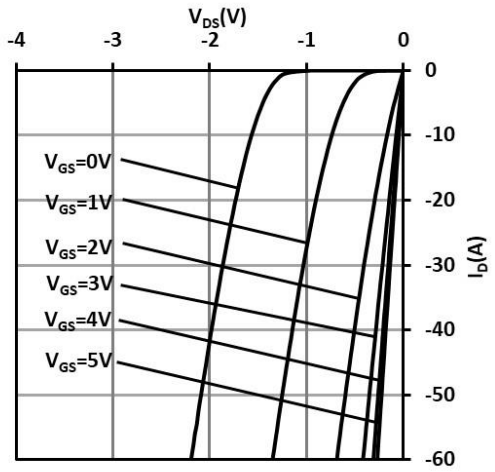


Fig. 9 Typ. Reverse Drain-Source Characteristics ($V_{GS}\leqslant 0$, T_J=125°C)

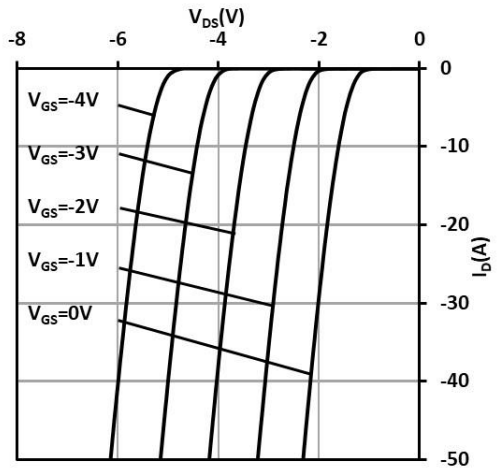


Fig. 10 Typ. Reverse Drain-Source Characteristics ($V_{GS}\geqslant 0$, T_J=125°C)

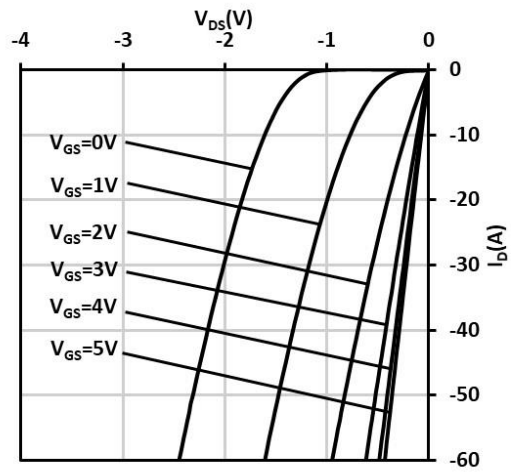


Fig. 11 Typ. Capacitances Characteristics

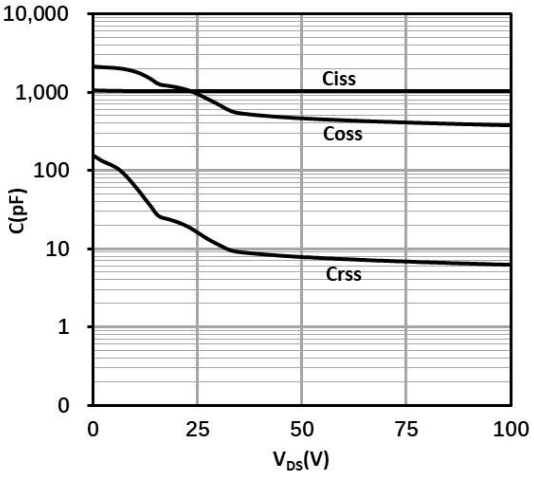


Fig. 12 Typ. Gate Charge

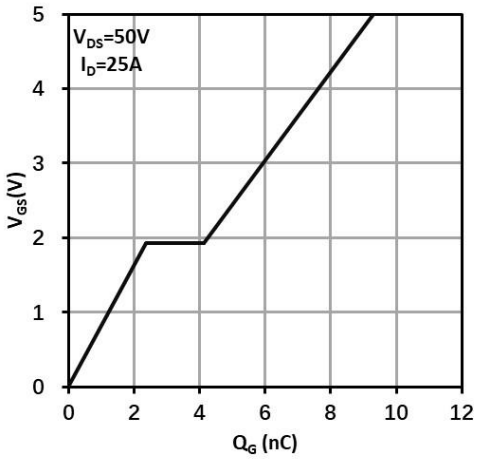


Fig. 13 Normalized Threshold Voltage vs. Temp.

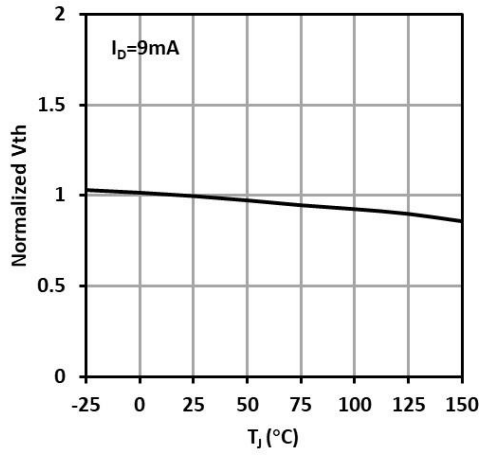


Fig. 14 Output Charge

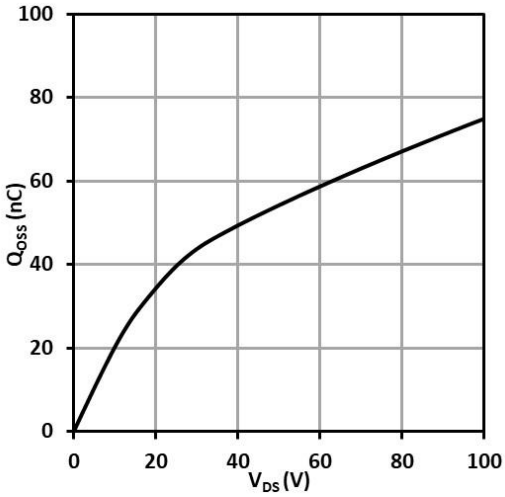


Fig. 15 Output Capacitance Stored Energy

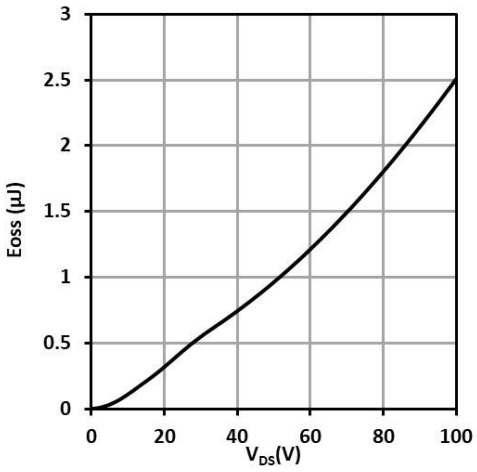


Fig. 16 Power Dissipation

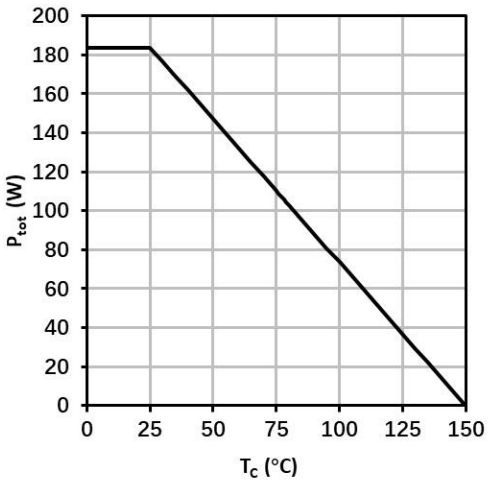


Fig. 17 Safe Operating Area

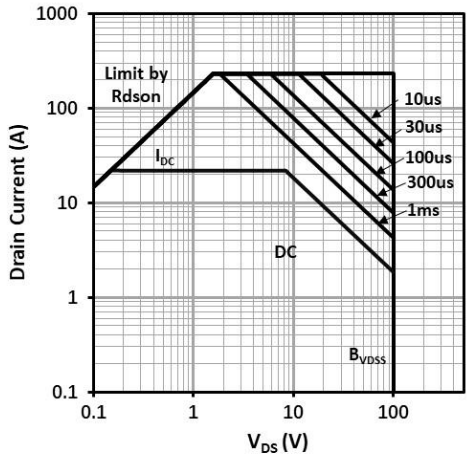
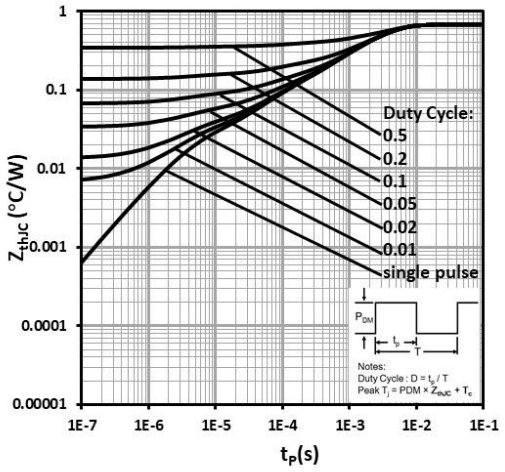
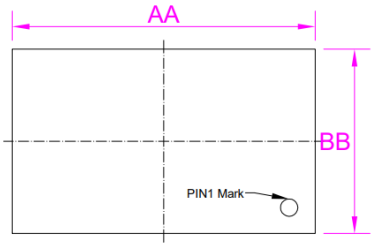


Fig. 18 Max. Transient Thermal Impedance

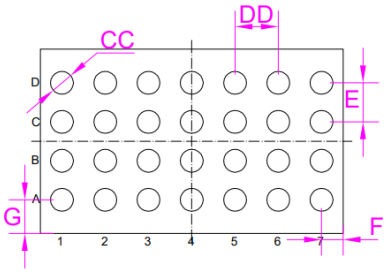


10. Package outlines

Package Reference

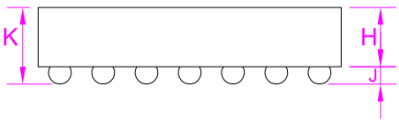


TOP VIEW



BOT VIEW

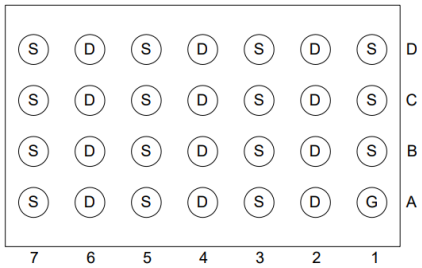
SYMBOL	MILLIMETER			NOTE
	MIN	NOM	MAX	
AA	3.473	3.498	3.523	
BB	2.103	2.128	2.153	
CC	0.237	0.264	0.291	28X
DD	0.50 BASIC			24X
E	0.45 BASIC			21X
F	0.249 REF			8X
G	0.389 REF			14X
H	0.671	0.685	0.699	
J	0.170	0.200	0.230	
K	0.838	0.885	0.932	



SIDE VIEW

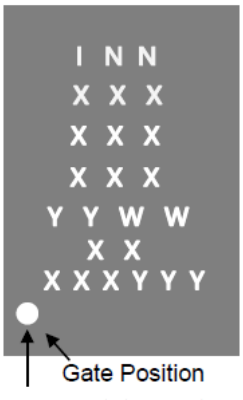
NOTE:
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.05 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-221.
4) DRAWING IS NOT TO SCALE.
5) A1 is Gate;
A2/A4/A6/B2/B4/B6/C2/C4/C6/D2/D4/D6 is Drain;
A3/A5/A7/B1/B3/B5/B7/C1/C3/C5/C7/D1/D3/D5/D7 is Source.

Pin Configuration:



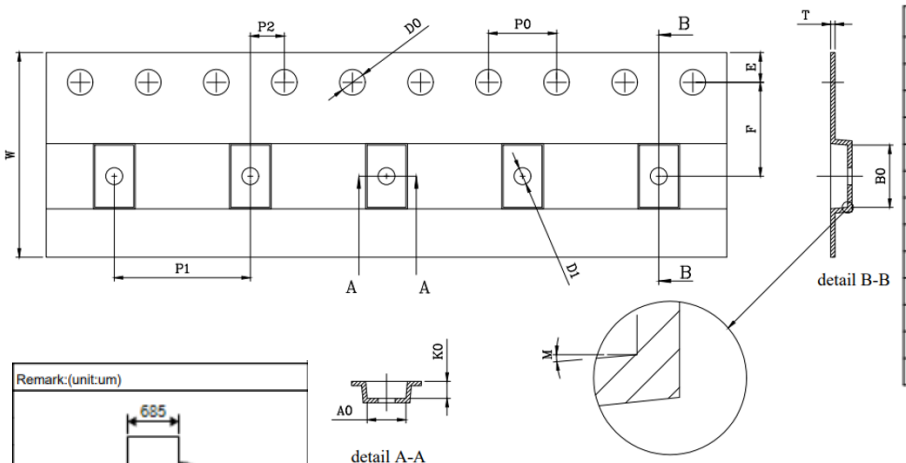
Top View

Marking Reference:

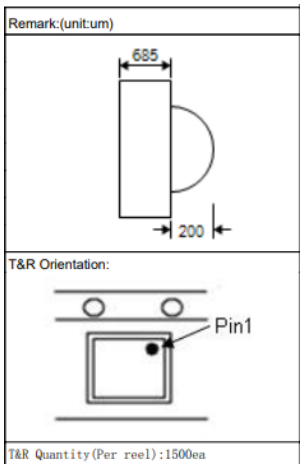


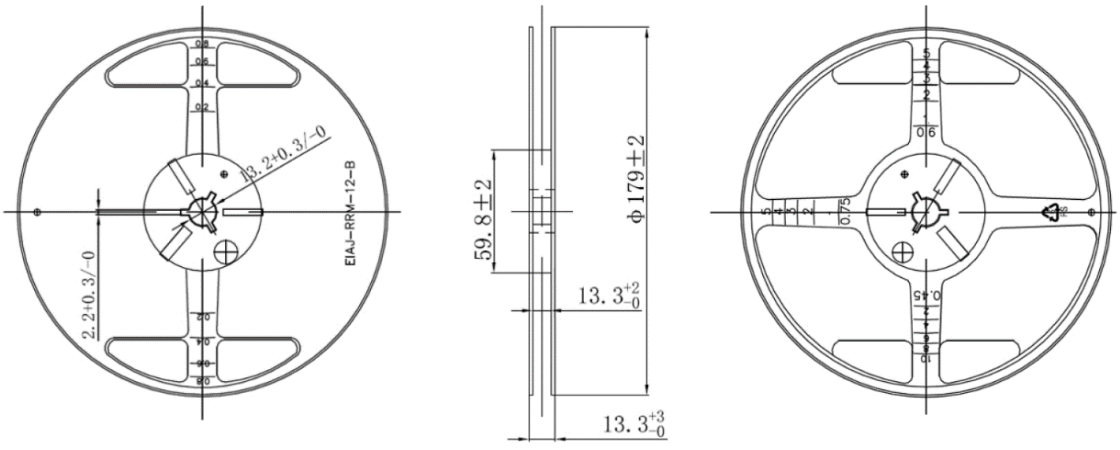
Row	Description	Example
Row1	Company name	INN
Row2	Product code	XXX
Row3	Lot Code	XXX
Row4		XXX
Row5	Date code	YYWW
Row6	Wafer ID	XX
Row7	Location ID	XXXYYY

11. Reel information



Item	Value&Tolerance
A0	2.28±0.05
B0	3.65±0.05
K0	1.00±0.05
D0	1.50+0.10/-0.00
D1	1.00±0.10
P0	4.00±0.10
P1	8.00±0.10
P2	2.00±0.05
E	1.75±0.10
F	5.50±0.05
T	0.25±0.03
W	12.00+0.30/-0.10
M	Max 5°

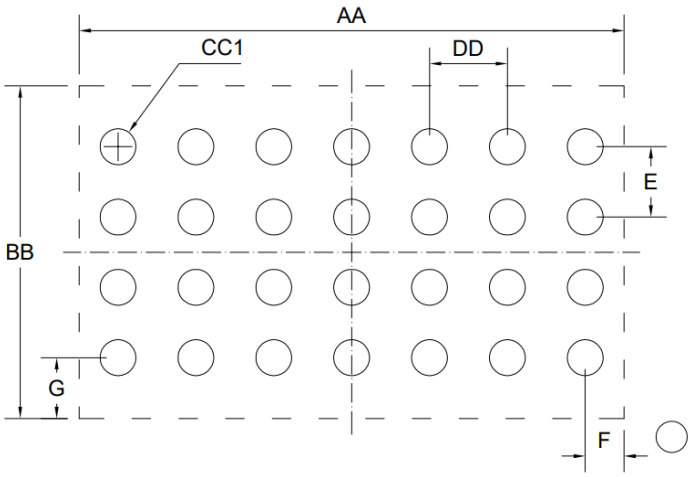




Note: units in mm.

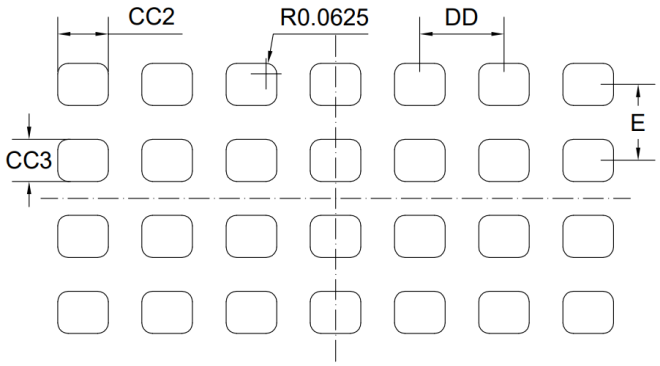
Land Pattern

Recommended Land Pattern



SYMBOL	MILLIMETER	NOTE
AA	3.498	
BB	2.128	
CC1	0.230	28X
DD	0.500	24X
E	0.450	21X
F	0.249	8X
G	0.389	14X

Recommended Stencil Drawing



SYMBOL	MILLIMETER	NOTE
CC2	0.300	28X
CC3	0.250	28X
DD	0.500	24X
E	0.450	21X

12. Revision history

Major changes since the last revision

Revision	Date	Description of changes
1.0	2024-11-08	Version 1.0 Release
1.1	2024-12-25	1. add Id,continue @Tc=25°C & Tc=125°C in table4; 2. update Fig. 4 & Fig. 5 in Electric characteristics diagrams.

Important Notice

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